Claim Amendments

Claim 1 (currently amended): A switch for a network comprising:

a plurality of fabrics~~, each fabric of the plurality of fabrics having~~:

a memory mechanism in which portions of packets as stripes are stored; and

a mechanism for instituting changes to the memory mechanism while the memory mechanism is continuously operating on the portions of the packets as stripes.

Claim 2 (original): A switch as described in Claim 1 wherein the memory mechanism includes a plurality of memory controllers.

Claim 3 (original): A switch as described in Claim 2 wherein the instituting mechanism includes a command buffer disposed in each memory controller in which changes to the memory controller are stored until the changes are implemented.

Claim 4 (previously presented): A switch as described in Claim 3 including a fabric in which the memory mechanism and the instituting mechanism are disposed, and

wherein the instituting mechanism includes an MCP (Module Control Processor) disposed in the fabric connected to the command buffer of each memory controller in the fabric, the MCP sends the changes to the buffer.

Claim 5 (previously presented): A switch as described in Claim 4 wherein each memory controller institutes changes in its command buffer at a same logical clock cycle when the memory controller receives an implementation signal.

Claim 6 (original): A switch as described in Claim 5 wherein the fabric has an aggregator which receives the implementation signal and sends it to the memory controllers.

Claim 7 (canceled)

Claim 8 (previously presented): A switch as described in Claim 6 including a port card which receives the implementation signal from the network and sends the implementation signal to each fabric in the switch.

Claim 9 (original): A switch as described in Claim 8 wherein the port card includes a striper and an unstriper, and the fabric includes a separator, the striper sending the

implementation signal to the aggregator of each fabric as a stripe, and the unstriper receiving any data from the separator of each fabric as a stripe.

Claim 10 (currently amended): A method for switching packets comprising:

storing portions of packets as stripes in a memory mechanism ~~of each fabric of a plurality of fabrics of a switch~~;

receiving changes for the memory mechanism of the switch having a plurality of fabrics at a buffer of the switch; and

implementing the changes to the memory mechanism when the memory mechanism receives an implementation signal while the memory mechanism continuously operates on the portions of the packets as stripes.

Claim 11 (previously presented): A method as described in Claim 10 wherein the memory mechanism includes a plurality of memory controllers with a memory controller of the plurality of memory controllers disposed in each fabric, and the buffer includes a command buffer disposed in each memory controller and the receiving step includes the step of receiving changes for each memory controller of each fabric at the command buffer.

Claim 12 (previously presented): A method as described in Claim 11 including before the receiving step, there is a step of sending the changes to each command buffer from a Module Control Processor of each fabric.

Claim 13 (original): A method as described in Claim 12 wherein the implementing step includes the step of implementing the changes to all the memory controllers of all the fabrics at a same logical clock cycle.

Claim 14 (previously presented): A method as described in Claim 13 including before the implementing step, there is a step of receiving the implementation signal at the switch in a receive message packets.

Claim 15 (previously presented): A method as described in Claim 14 wherein the implementation signal receiving step includes the step of receiving the receive message packet at a port card of the switch.

Claim 16 (previously presented): A method as described in Claim 15 including after the packet receiving step, there is a step of sending the implementation signal using a striper of the port card as a stripe to an aggregator of each fabric of the switch.

Claim 17 (previously presented): A method as described in Claim 16 including after the implementation sending step, there is a step of transferring the implementation signal from the aggregator to each memory controller.